X and Ku Band High Efficiency Power GaAs FETs

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ABSTRUCT

New structual,high productive power GaAs FETs have been developed,achieving power added efficiency ranging from 30 % to 40 % with 1.5 W power output between 10 to 15.2 GHz on mass production basis. Internally matched devices with two chips have exhibited the supreme performance of 3 W power output with as high as 40 % power added efficiency at 15.2 GHz. These devices have structual features on the 0.5 μm deep recessed gate utilizing photoresist-free gate formation and the sidewall metallization combined with PHS and via hole structure.

INTRODUCTION

The communication systems using low noise and power GaAs FETs are increasing rapidly. In these systems,power added efficiency as well as output power is an important factor to minimize sizes and dissipation power of the equipments. In order to achieve high efficiency GaAs FET on mass production basis,device parameters and fabrication technologies have to be optimized considering both performances and productivity. The power GaAs FETs designed on basis of these objectives have exhibited power added efficiency as high as 40 % up to 15.2 GHz.

DEVICE DESIGN

In order to achieve high power added efficiency, both high saturation power and high associated gain are inevitable.

To accomplish high saturation power,it is important to reduce the source series resistance(R_s), to reduce the thermal resistance(R_{th}) and to keep breakdown voltage(BV_{gd}) high. A deep recessed gate structure has been adopted to reduce the R_s. The recess width was optimized to ensure both low R_s and high BV_{gd}. The PHS structure has been utilized torealize low R_{th}.

On the other hand, low source inductance(L_s),low gate-to-source and gate-to-drain capacitance(C_{gs},C_{gd}) and large transconductance(g_m) are necessary to accomplish high gain performance. In order to reduce C_{gs} and C_{gd}, gate length(L_g) should be reduced as fine as possible. By compromizing the performance and the mass productivity, the gate length was defined to be 0.5 μm. Impurity concentration(1.5×10^{17} cm^{-3}) and recess width(2.5 μm) were determined after experimental optimization[1] giving high g_m,low R_s and high BV_{gd}. For high cut off frequency devices,much attention should be paid to reduce source inductance.[2][3] In addition to via hole structure,sidewall metallization has been utilized to reduce source inductance. The source inductance was reduced to two-thirds by adding the sidewall metallization.

DEVICE FABRICATION

The developed FET,consisting of 75 μm gate fingers, has the total gate width of 3mm.(Fig.1)

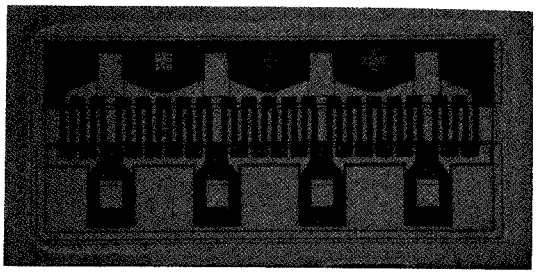

Fig.1 Top view of the GaAs FET chip,measuring 1.0 mm x 0.5 mm

The device fabrication has two features of photoresist-free gate formation and the combination of PHS, via hole and sidewall metallization.

Ti/Al gate is formed in the deep recess region by applying lift-off process,utilizing SiO_2-Si_3N_4 double layer as a lift-off material instead of conventional photoresist. This photoresist-free gate formation ensures stable Schottky barrier.

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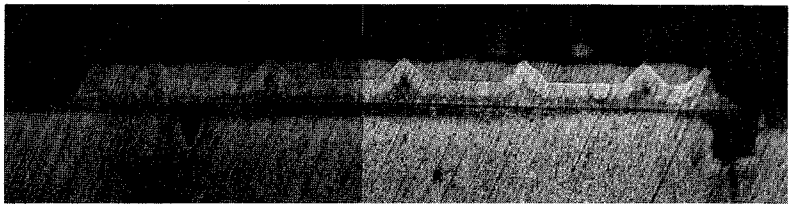

Fig.2 crosssection of the developed FET

In the PHS and via hole process, GaAs substrate is chemically etched off from the bottom to the upper source pads. Then chip sidewall as well as chip bottom is simultaneously gold plated by 30 μm.This sidewall metallization favours durability against mechanical and thermal shocks,giving a remarkable improvement in the productivity in assembling. As shown in Fig.2, plated gold covers chip sidewall as well as chip bottom and holes. Solder is well attached to the plated gold,guaranteeing a low thermal resistance between them. With this PHS structure,thermal resistance is reduced drastically to 9°C/W from 22°C/W. The thermal resistance distribution of the 3mm devices is shown in Fig.3, in which conventional FETs' thermal resistance is also shown for comparison.

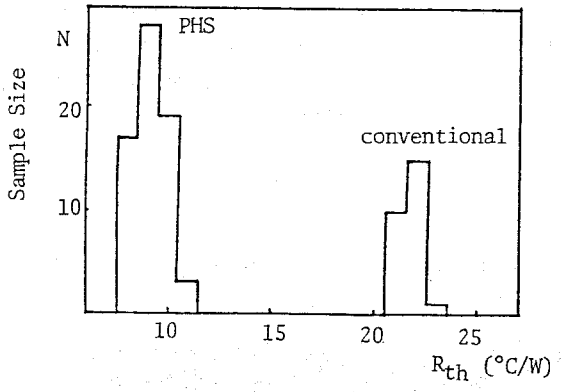

Fig.3 Thermal resistance distributions of the developed FETs and of the conventional FETs with 140 μm GaAs substrate

DC AND RF PERFORMANCES

Fig.4 illustrates the typical DC characteristics of the developed FET. With the deep recessed gate structure,the transconductance is as high as 110 mS/mm.

Fig.5 shows the relationship between power added efficiency and frequency measured on the developed devices. As a result of the combination of high transconductance,reduced source inductance,reduced source resistance and reduced thermal resistance,the 3mm devices have exhibited 1.5W power output with power added efficiency as high as 40 % up to 15.2 GHz. The device has a chip condenser for input matching circuit. The RF performances were measured with Alford twin sleeve tuners.

The internally matched 6mm device,including two 3mm gate width chips,is hermetically sealed in a metal package. The RF performances were measured by utilizing the special jig, which connected FET's leads to a 50-ohm coaxial line directly without any additional circuit. FET biasing was done through the bias-tee.

Input/output power responses of the 6mm device, whose matching circuit was designed for 15 GHz,are shown in Fig.6.The device exhibited 3W power output with 5.7 dB associated gain, 40 % power added efficiency and 7.5 dB linear gain at 15.2 GHz.

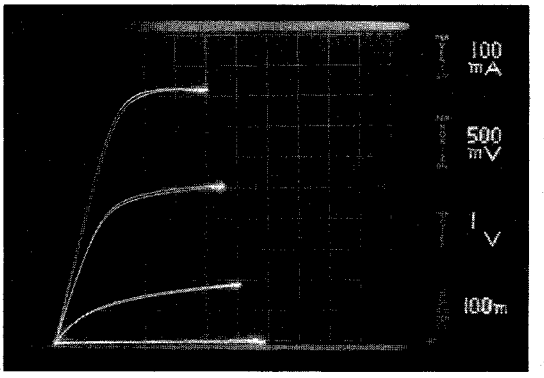

Fig.4 Drain current v.s. drain-to-source voltage characteristics
(total gate width : 3mm)

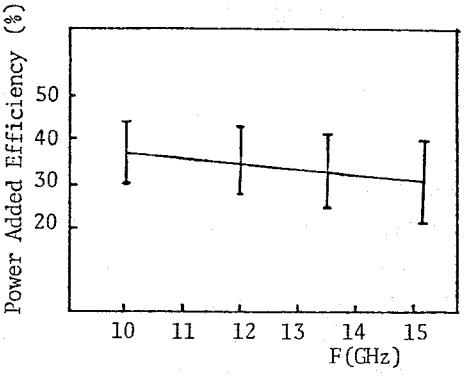

Fig.5 Power added efficiency v.s. frequency

In comparison with 'K and Ka Band Power GaAs FET'[1], linear gain is improved by about 2 dB and saturation power is improved by 1 dB as shown in Table 1. The improvement of saturation power is attributed mainly to the reduced channel temperature and increased drain current by PHS structure and the improvement of linear gain mainly to the reduced source inductance by via hole structure.

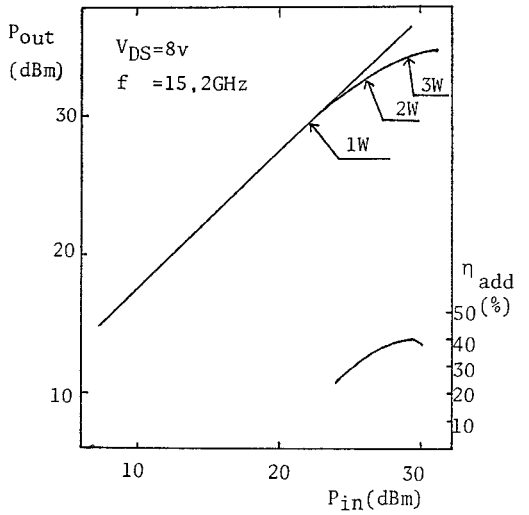

Fig.6 Input/output power responses of the 6mm device at 15.2 GHz

	P_{sat}	G_L	η_{add}	R_S	C_{gs}	g_m	L_S	R_{th}	BV_{gd}
A	32	8.5	40	0.8	3.6	110	16	9	14
B	31	6.5	28	0.9	3.6	110	45	22	13
unit	dBm	dB	%	Ω	pF	mS/mm	pH	°C/W	V

Table 1 Comparison of typical device parameters and RF performances at 13.5 GHz
A : developed FETs
B : conventional FETs with the same structure except PHS and via hole

CONCLUSION

0.5 μm-gate, high performance power GaAs FETs, appropriate for mass productivity, have been developed by introducing both the deep recessed gate structure and the sidewall metallization combined with PHS and via hole. By this structure, device parameters such as C_{gs}, C_{gd}, g_m, L_s, R_{th} are sufficiently improved. Especially, massive reduction of Ls and R_{th} resulted in power added efficiency ranging from 30 to 40 % up to 15.2 GHz. The internally matched FETs of 3W power output exhibited a supreme performance of 40 % power added efficiency at 15.2 GHz.

ACKNOWLEDGEMENT

The authors thank Dr.T.Irie, Dr.K.Sekido, Mr.N.Kitagawa, Mr.H.Horikiri, Mr.M.Ayusawa and Mr.M,Kondo for their supports on this work and warm encouragement. They are also grateful to Dr.Y.Higashisaka, Mr.Y.Aono, Mr.Y.Hirakawa, Mr.M.Nakajima, Mr.A.Mochizuki, Mr.S.Nakao, Mr.K.Nagai and Mr.K.Katsukawa for their helpful discussions.

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